CLAIMS

What is claimed is:

1. A semiconductor assembly comprising:

a carrier substrate having conductive pads exposed on a surface thereof;

a semiconductor substrate adjacent the carrier substrate and having an active surface and a back surface, the active surface having bond pads exposed thereon;

a plurality of wire bonds extending between bond pads of the semiconductor substrate and conductive pads of the carrier substrate;

a plurality of spaced adhesive elements disposed in an area of overlap between a face of the carrier substrate and an opposing surface of the semiconductor substrate; and

a volume of dielectric filler material disposed between adjacent spaced adhesive elements in the area of overlap and bonding the semiconductor substrate to the carrier substrate.

2. The semiconductor assembly of claim 1, wherein the carrier substrate comprises a first surface, a second surface and an opening extending through the carrier substrate therebetween, the second surface having the conductive pads exposed thereon, the semiconductor substrate located over the first surface of the carrier substrate so that the bond pads are exposed through the opening and the wire bonds extend through the opening between the bond pads and the conductive pads.

3. The semiconductor assembly of claim 1, wherein the plurality of spaced adhesive elements comprises a substantially symmetrical adhesive element arrangement.

4. The semiconductor assembly of claim 1, wherein the plurality of spaced adhesive elements comprises adhesive point pads mutually separate and discrete from each other.

5. The semiconductor assembly of claim 4, wherein at least some of the spaced adhesive point pads are positioned proximate at least corner portions of the semiconductor substrate.

6. The semiconductor assembly of claim 5, wherein at least some of the spaced adhesive point pads are positioned proximate at least one peripheral edge of the semiconductor substrate.

7. The semiconductor assembly of claim 1, wherein the plurality of spaced adhesive elements comprises elongated pads mutually separate and discrete from each other.

8. The semiconductor assembly of claim 2, wherein the plurality of spaced adhesive elements comprises elongated pads mutually separate and discrete from each other.

9. The semiconductor assembly of claim 8, wherein the elongated pads are positioned laterally adjacent the opening and extend substantially parallel to the opening.

10. The semiconductor assembly of claim 8, wherein the elongated pads are positioned laterally adjacent the opening and extend substantially transverse to the opening.

11. The semiconductor assembly of claim 1, wherein the dielectric filler material coats or encapsulates at least portions of at least some of the wire bonds.

12. The semiconductor assembly of claim 11, further comprising a volume of dielectric encapsulation material extending over at least exposed portions of wire bonds having portions coated or encapsulated by the dielectric filler material.

13. The semiconductor assembly of claim 12, further comprising a volume of dielectric encapsulation material extending over at least a majority of the semiconductor substrate.

14. The semiconductor assembly of claim 1, wherein the dielectric filler material substantially fills a standoff between the semiconductor substrate and the carrier substrate.

15. The semiconductor assembly of claim 1, wherein the spaced adhesive elements comprise at least one of a decal, a tape segment and a volume of adhesive.

16. The semiconductor assembly of claim 1, wherein the semiconductor substrate comprises one or more semiconductor dice.

17. The semiconductor assembly of claim 1, wherein the carrier substrate comprises at least one of a BT resin, a ceramic material, a polymeric material, FR-4 material and FR-5 material.

18. The semiconductor assembly of claim 1, wherein the carrier substrate comprises a first surface and a second surface, the first surface having the conductive pads exposed thereon, the back surface of the semiconductor substrate located over the first surface of the carrier substrate.

19. An electronic system comprising:

a processor device coupled to an input device and an output device; and

a semiconductor assembly coupled to at least one of the processor device, the input device and the output device, the semiconductor assembly comprising:

a carrier substrate having conductive pads exposed on a surface thereof;

a semiconductor substrate adjacent the carrier substrate and having an active surface and a back surface, the active surface having bond pads exposed thereon;

a plurality of wire bonds extending between bond pads of the semiconductor substrate and conductive pads of the carrier substrate;

a plurality of spaced adhesive elements disposed in an area of overlap between a face of the carrier substrate and an opposing surface of the semiconductor substrate; and

a volume of dielectric filler material disposed between adjacent spaced adhesive elements in the area of overlap and bonding the semiconductor substrate to the carrier substrate.

20. The electronic system of claim 19, wherein the carrier substrate comprises a first surface, a second surface and an opening extending through the carrier substrate therebetween, the second surface having the conductive pads exposed thereon, the semiconductor substrate located over the first surface of the carrier substrate so that the bond pads are exposed through the opening and the wire bonds extend through the opening between the bond pads and the conductive pads.

21. The electronic system of claim 19, wherein the plurality of spaced adhesive elements comprises a substantially symmetrical adhesive element arrangement.

22. The electronic system of claim 19, wherein the plurality of spaced adhesive elements comprises adhesive point pads mutually separate and discrete from each other.

23. The electronic system of claim 22, wherein at least some of the adhesive point pads are positioned proximate at least corner portions of the semiconductor substrate.

24. The electronic system of claim 22, wherein at least some of the adhesive point pads are positioned proximate at least one peripheral edge of the semiconductor substrate.

25. The electronic system of claim 19, wherein the plurality of spaced adhesive elements comprises elongated pads mutually separate and discrete from each other.

26. The electronic system of claim 20, wherein the plurality of spaced adhesive elements comprises elongated pads mutually separate and discrete from each other.

27. The electronic system of claim 26, wherein the elongated pads are positioned laterally adjacent the opening and extend substantially parallel to the opening.

28. The electronic system of claim 26, wherein the elongated pads are positioned laterally adjacent the opening and extend substantially transverse to the opening.

29. The electronic system of claim 19, wherein the dielectric filler material coats or encapsulates at least portions of at least some of the wire bonds.

30. The electronic system of claim 29, further comprising a volume of dielectric encapsulation material extending over at least exposed portions of wire bonds having portions coated or encapsulated by the dielectric filler material.

31. The electronic system of claim 30, further comprising a volume of dielectric encapsulation material extending over at least a majority of the semiconductor substrate.

32. The electronic system of claim 19, wherein the dielectric filler material substantially fills a standoff between the semiconductor substrate and the carrier substrate.

33. The electronic system of claim 19, wherein the spaced adhesive elements comprise at least one of a decal, a tape segment and a volume of adhesive.

34. The electronic system of claim 19, wherein the semiconductor substrate comprises

one or more semiconductor dice.

35. The electronic system of claim 19, wherein the carrier substrate comprises at least one of a BT resin, a ceramic material, a polymeric material, FR-4 material and FR-5 material.

36. The electronic system of claim 19, wherein the carrier substrate comprises a first surface and a second surface, the first surface having the conductive pads exposed thereon, the back surface of the semiconductor substrate located over the first surface of the carrier substrate.

37. A semiconductor assembly comprising:

a semiconductor substrate attached to a carrier substrate with a plurality of mutually spaced elements disposed in an area of overlap between a surface of the semiconductor substrate and an opposing surface of the carrier substrate and a plurality of wire bonds extending between the semiconductor substrate and the carrier substrate; and

a volume of dielectric filler material disposed between adjacent mutually spaced elements in the area of overlap providing a predominant portion of a bond between the semiconductor substrate and the carrier substrate.

38. The semiconductor assembly of claim 37, wherein the dielectric filler material surrounds at least portions of at least some of the wire bonds.

39. The semiconductor assembly of claim 38, further including a dielectric encapsulation material at least encapsulating exposed portions of the at least some of the wire bonds.

40. The semiconductor assembly of claim 37, wherein the wire bonds extend through an opening in the carrier substrate.

41. The semiconductor assembly of claim 40, wherein the dielectric filler material

surrounds at least portions of at least some of the wire bonds.

42. The semiconductor assembly of claim 41, further including a dielectric encapsulation material at least encapsulating exposed portions of the at least some of the wire bonds.